ASTEELFLASH
YOUR EMS PARTNER

PCB GENERIC REQUIREMENTS

QUALITY ASSURANCE REQUIREMENTS FOR PCB SUPPLIERS

Version	Date	Writing	Object of evolution	Verification	Approval
3	20/12/2018	L. LE BERRE	Release	E. GIRAULT T. AZEVEDO S. KOETTEL	V. PRADIA
2.6	29/10/2018	L. LE BERRE	Modification §10.2 : Type of packaging	E. GIRAULT T. AZEVEDO S. KOETTEL	V. PRADIA
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1	10/01/2011	V. CHASSAIN	Creation of EMA_WI_ENG_001 : PCB General Requirement	D. MAWAS	D. MAWAS

English Version

Composition of the review committee:

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1. PURPOSE

The object of his specification it to define the procurement of the printed circuit boards, for the following technologies:

- Rigid board
- Rigid-Flex board
- Flex-board

2. SUMMARY

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3. STANDARDS

ANSI/IPC-SM-840	Qualification and Performance specification of permanence solder mask
IPC 4562	Metal Foil for Printed Board Applications
IPC-2221	Generic Standard on Printed Board Design
IPC-2222	Sectional Standard on Rigid Organic Printed Boards
IPC-2223A	Sectional Design Standard for Flexible Printed Boards
IPC-2226	Sectional Design Standard for HDI Printed Boards
IPC-4101	Specification for Base. Materials for Rigid and Multilayer Printed Boards
IPC-4550	General Specification for PCB Surface Finishes
IPC-4552	Specification for Electroless Nickel/immersion Gold (ENIG) Plating for PCB's
IPC-4554	Specification for chemical Tin
IPC-4562	Metal Foil for Printed Board Applications
IPC-4761	Design Guide for Protection of Printed Board Via Structures
IPC-6011	Generic Performance Specification for Printed Boards
IPC-6012	Qualification and Performance Specification for Rigid Printed Boards
IPC-6012DA	Automotive Applications Addendum Qualification and Performance Specification for Rigid Printed Boards
IPC-6013	Qualification and Performance Specification for Flexible Printed Boards
IPC-6015	Qualification and Performance Specification for Organic Multichip Module Mounting and Interconnecting Structures
IPC-6016	Qualification and Performance Specification for High Density Interconnect (HDI) Layers or Boards
IPC-6018	Microwave End Product Board Inspection and Test
IPC-7721	Repair and Modification of Printed Boards
IPC-9252	Guideline for requirements for electrical testing for unpopulated circuit board
IPC-A-600	Acceptability of Printed Boards
IPC-MC-324	Performance Specification for Metal Core Boards
IPC-ML-960	Qualification and Performance for Mass Lamination Panels for Multilayer Printed Boards
IPC-TF-870	Qualification and Performance of Polymer Thick Film Printed Boards
IPC-TM-650	Test Method Manual
J-STD-003	Solderability Test for printed Board

4. APPLICABLE DOCUMENTS

Following hierarchy is binding:

1. Customer files & Specifications
2. Asteelflash PCB Generic Requirement & Specification sheet
3. Norms/standards

The supplier must ensure that deviations from the requirements of the contract or order are communicated, shared with the customer and resolved.

NB: The supplier should perform a manufacturability analysis (eg. DFM (Design for Manufacturing)…) for all new PCB before the start of production. Any deviation identified must be formalized through an official document (eg. EQ ...)

5. ASTEELFLASH GROUP SPECIFICATIONS

5.1 PCB SURFACE FINISHES

Find below PCB surface finishes thickness required by Asteelflash and IPC recommendations for information only.

	Thickness	
Surface Finish	**Asteelflash requirements**	IPC requirements (IPC 6012/6013/6018) for information only
HASL Lead free (SAC or Sn100C)/ pb	**100% solderable and wetting** **0,5 µm – 40 µm (wetting: 100%)**	100% solderable and wetting
Immersion tin	**100% solderable and wetting** **>= 1,0 µm (wetting: 100%)**	100% solderable and wetting
Immersion Silver	**100% solderable and wetting** **AABUS (As Agreed Upon Between User and Supplier.)**	100% solderable and wetting
ENIG (Electroless Ni / Immersion Au) / Gold plating)	**Au: 0,05 µm - 0,12 µm** **Ni: 3µm - 7 µm**	Au 0,05 µm - 0,12 µm Ni > 3 µm
Electrolytic gold (hard gold) Plug contact e.g. keyboard base	**1,25µm>= Au >= - 3 µm** **Ni: 4-7 µm**	Au > 0,8 µm (Class 2) or > 1,25 µm (Class 3) Ni > 2,5 µm
Electrolytic gold (gold wire bonding)	**Thermosonic bonding: Au: 0,8 µm - 1,5 µm** **Ultrasonic bonding: 0,5 - 1 µm** **Ni: 4- 7 µm** **Use pure gold (99,9%)**	Thermosonic bonding: Au: > 0,3 µm (Class 2) or > 0,8 µm (Class 3) Ultrasonic bonding: Au: > 0,05 µm Ni > 3 µm
Electrolytic gold(SMT pads)	**Au: 0,12 µm - 0,25 µm** **Ni : 3 µm - 7 µm**	Au < 0,45 µm Ni > 3 µm
Flash Gold	**Au 0,05 µm - 0,12 µm** **Ni: 3 µm - 7 µm**	Au 0,05 µm - 0,12 µm Ni > 1,2 µm
OSP / Passivation	solderable 0,3 – 0,5µm	solderable

The exact value of the thickness should be notified by Asteelflash or Asteelflash's customer in the specification PCB sheet.

5.2 PCB IDENTIFICATION

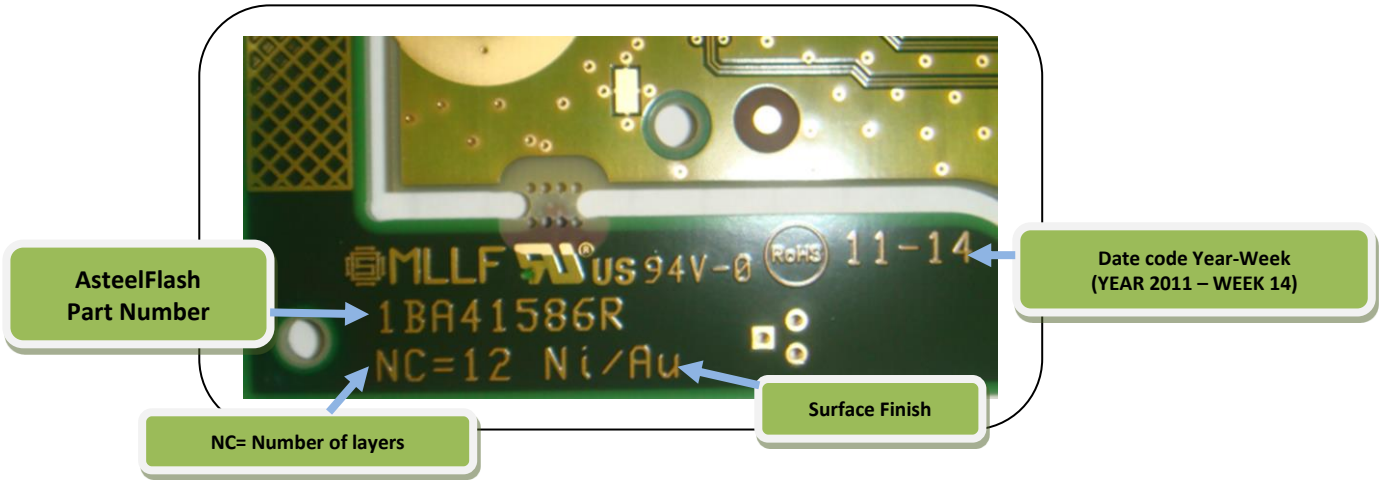
5.2.1 **Identification**

- On Unit PCB

  Each batch is a homogeneous production (all manufacturing conditions being identical). Batch is identified with its date code marked on all unit PCB's (YY-WW: year week [example: 16-33, week 33 of year 2016]), plus following information if specified in the PCB specification sheet: UL marking, manufacturer's logo, RoHS marking, 2D marking…

- On the technical area (break away tab)

  This information could exist on the panelization drawing provided.
  Each technical area should mention the following information :



5.2.2 **Date code**

At the incoming, the date code of PCB must be in accordance with the information notified below:

Surface Finish	Expiry date	Incoming date code PCB supplier and Asteelflash site in the same region : EMEA to EMEA / APAC to APAC/ AMER to AMER	Incoming date code PCB supplier and Asteelflash site in different region : APAC to EMEA / APAC to AMER / ….
HAL lead free or Sn Pb	12 months	< 2 months	< 4 months
ENIG (Electroless Ni / Immersion Au)	12 months	< 2 months	< 4 months
Electrolytic Gold(Ni /Au)	36 months	< 26 months	< 26 months
Immersion tin	6 months	< 2 months	< 2 months
OSP	6 months	< 2 months	< 2 months
Immersion silver	6 months	< 2 months	< 2 months

Nevertheless, a deviation can be subjected to AsteelFlash, mentioning the number of layers, date code, solderability test conditions (methods, bath…). Panels should be identified and must be isolated from the rest of the shipping and a solderability test must be provided.

NB: Beyond the expiry date:

- For the immersion Ni-Au finish: circuit boards can be deoxidized one time. They have so to be soldered into the next 2 weeks. Only one reactivation is allowed.
- For the immersion tin finish: the stripping is not allowed and PCB have to be scrapped.

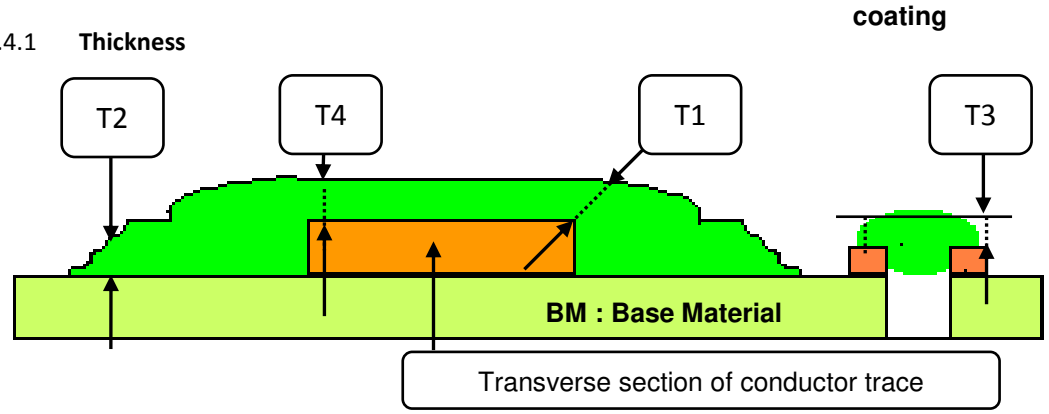
Reminder: Tin finished circuit board must be stored in a temperature controlled environment. The temperature must not exceed 25°C

5.3 DRILL TOLERANCE

Drill tolerance is specified in the PCB specification sheet. If not, unplated holes, tolerance is +/- 0,05mm for all diameters.

5.4 SOLDER MASK

5.4.1 Thickness



T1 = on conductor edge	> 5 µm
T2 = on base material	15 µm < T < 45 µm
T3 = on via through connection (via)	< 45 µm
T4 = on conductor surface	< 45 µm

5.4.2 Material

Solder masks must correspond with IPC-SM-840 Class H

The solder marks must be compatible with the conformal coating material which could be used on the PCBA (surface tension) and specified in the PCB data.

5.4.3 Vias protection

Via protection specifications must correspond to IPC-4761.

5.4.4 Test points

According to IPC 6012, chapter 3.7.1.e, test points should be free of solder mask unless coverage is specified.

5.5 CLEANLINESS – IONIC CONTAMINATION

5.5.1 Cleanliness

Before packaging, circuit board must be cleaned to avoid any residues, dust, finger print and any contaminants.

5.5.2 Ionic contamination

The solvent resistivity shall be done in accordance with IPC-6010 series unless otherwise specified. The specimens shall be tested for ionic contamination in accordance with IPC TM 650 chap 2.3.25 and 2.3.26.

5.6 METALLOGRAPHIC CROSS SECTION

Coupon must be representative of the circuit board (diameter of the smallest holes, areas with high density of vias [ratio the most important], diameter of the vias which predominates, diameter of the plugging holes which predominates in the circuit board). This cut must be identified with the AsteelFlash Group code and the date code.

The result of the cross section, before and after thermal shock, must be integrated into the PCB report.

6. BASE MATERIALS

Base materials are the ones characterized in IPC 4101 - datasheets 99, 124, 126 and 129.

Without any specific requirements, AsteelFlash Group requires:

TECHNOLOGY	IPC4101 Data Sheet Requirement			
	99	124	126	129
Criteria 1 : IPC-A-600 Class 1 or 2 Or **Criteria 2** : File customer request a minimal Tg of 140°C Or **Criteria 3** : PCB with < 8 layers	VALIDATED			
Criteria 1 : : IPC-A-600 Class 3 Or **Criteria 2** : File customer request a minimal Tg of 170°C Or **Criteria 3** : PCB with buried or blind via, sequential build up or semi sequential build up Or **Criteria 4 :** PCB with xBGA or shielding Or **Criteria 5:** Controlled impedances Or **Criteria 6:** Fine pitch components 0.5mm Or **Criteria 7 :** 1 Mhz >Frequency > 1 Ghz	NOT VALIDATED		VALIDATED	
Criteria 1 : : IPC-A-600 Class 3 Or **Criteria 2** : File customer request a minimal Tg of 170°C Or **Criteria 3** : PCB with buried or blind via, sequential build up or semi sequential build up Or **Criteria 4 :** PCB with xBGA or shielding Or **Criteria 5:** Controlled impedances Or **Criteria 6:** Fine pitch components 0.5mm Or **Criteria 7 :** 1 Ghz > Frequency > 10 Ghz	NOT VALIDATED			VALIDATED

If the base material provided is not following these datasheets, the supplier should submit a deviation request to AsteelFlash for approval.

In any case, the supplier must provide to AsteelFlash the name and reference of base material.

Mix of base material is forbidden.

NB: for single or double face boards, supplier is able to propose another base material with lower specification (Tg > 130°C, datasheet 92, 93).

Furthermore, base copper must be HTE.

7. REPAIRS

Repairs are allowed only after agreement from Asteelflash. In this case only :

- Printed circuit board repairs have to be made per according IPC 7721.
- PCB must be identified and the repair must be localized on the PCB.
- Nevertheless, repairs are prohibited on the internal layers.

Solder mask retouches are allowed and should fulfill the following conditions:

- Conformity with IPC 7711/21
- Adherence or repaired area is conform to IPC-TM-650 requirements
- Material used for retouch is compatible with the solder mask processed on circuit
- The repair doesn't affect surface aspect for SMT component assembly

8. PANELS

8.1 DEFECTIVE BOARDS IN PANEL

No panel accepted with a circuit defect.

The admission of individual defective circuit boards in a multiple pattern is subject to agreement with the respective ASTEELFLASH GROUP locations.

Marking of every defective individual PCB is implemented at the specified positions (mainly register guides or changeover pads) with a dark, matt and round cover > 4.0 mm and crossed out in diagonals. This cover must be temperature and solder wave proof (260°C) as well as resistant to ultrasound cleaning. The diameter of the round cover must cover off around the available markings for at least 2 mm, whereby no circuit board multiple pattern scribing, SMD pad´s or parts of neighboring "good" individual PCBs may be affected. With double-sided SMD component mounting, both PCB sides of the reject PCB should be marked.

Caution: All defective PCB multiples should be packed separately for delivery. The packaging of the PCB multiples with the defective PCBs must be clearly marked.

8.2 DECENTERING:

For multipanel set up, following tolerances have to be respected:

- Picture/picture decentering : +/- 0,076mm
- Hole/hole decentering : +/- 0,076mm

9. TEST

9.0 AOI

All internal layers have to be controlled, 100%, with AOI equipment.

9.1 ELECTRICAL TEST

Electrical test have to be performed on all the circuits. Parameters to test are :

- Continuity of all the equipotential
- Isolation of one equipotential with all the others.

Isolation and continuity shall be conform to IPC 9252.

Supplier marks PCB with a black line on PCB edge.

10. PACKAGING

10.1 PACKAGING RULES

a) The circuit boards with the respective ordering quantity should be delivered with a maximum of 30 panels per packaging unit, containing individual circuit boards or multiple patterns in the following ESD packaging (unless otherwise agreed)
b) Common orientation of all PCBs in a packaging unit
c) Only circuit boards from a single manufacturing batch may be included in a packaging unit
d) Date code, part count and article number must be printed on every packaging unit.
e) In all cases, the packaging material must be chemically neutral, free of silicone release agents and may not adhere to the circuit boards. For packaging materials, the statutory packaging regulations (regulations for the avoidance of packaging and waste) shall be used.
f) The package shall avoid any risk of friction between the boards.
g) Packaging units with a weight > 15 kg may not be used. For this purpose, fewer circuit boards can be combined to form a packaging unit. Exceptions are only possible after prior consultation with ASTEELFLASH GROUP.
h) In general: no use of intermediate layers. Exception: carbon, flex-mask, metal

10.2 TYPE OF PACKAGING

FINISH / TYPE	Dry pack	Vacuum Plastic (Shrink foil)
Immersion Tin (Sn)	Allowed	Allowed
Immersion Silver (Ag)	Allowed	Allowed
OSP	Mandatory	Forbidden
ENIG (Ni Au)	Allowed	Allowed
Tin Lead	Allowed	Allowed
Flex-board (All finish)	Recommended	Allowed

10.2.1 **Dry Pack**

a) Circuits shall be packed into a chemically inert heat-sealed polyethylene film (any ionic or organic contaminant must be outgassed)
b) The package must contain a desiccant bag and a humidity indicator (with a minimum at 5% RH) put on the side of PCB (no desiccant in contact with the circuits)
c) Supplier must ensure an outgassing of the circuits before packaging. Outgassing conditions are under the supplier responsibility.

10.2.2 **Vacuum Plastic (Shrink foil)**

a) This shrink foil is equipped with antistatic agent and can be classified as isolating according ESD directive.
b) The package must contain a desiccant bag and a humidity indicator (with a minimum at 5% RH) put on the side of PCB (no desiccant in contact with the circuits)
c) Special versions are possible after consultation with ASTEELFLASH.

10.3 IDENTIFICATION

In all cases, don't mix into the package:
- Different date codes
- Panel with a nonconforming circuit
- PCB under dispensation
- PCB repaired

All panels must be oriented in the same direction in the package

Each package must be labeled with the following information:
- AsteelFlash Group Purchase Order (PO)
- AsteelFlash Group part number & revision/version
- Supplier part number
- Manufacturer name
- RoHS yes/no
- Quantity
- Number of batch
- Date code
- Surface finish
- Asteelflash Deviation number (if applied)

Note: Samples & non-conform PCB under deviation shall be packed in a separate packaging unit and clearly identified on the packaging

11. HANDLING AND TRANSPORTATION PRECAUTIONS

In order to avoid any deterioration during handling and transportation, a rigid plate must be placed above and below the stack for the following PCB:
- Flex
- PCB with thickness is less or equal to 1,2 mm
- PCB with paper raw material (CEM, FR1, FR2 …)

The supplier must take all dispositions in order to keep mechanical and electrical specification, as well as visual aspect, during the transport (among others things, to avoid any movement between circuits).

It is prohibited to handle the boards with bare hands, if possible, they have to be taken at the board edges in order to avoid contact of gloves with the SMT pads.
- Gloves are mandatory to handle the PCB
- PCB must be handle by edges
- Contact with PCB surface is mandatory

12. CONTROL AND DOCUMENTATION

12.1 ACCEPTABILITY LEVEL

Visual control must be done at 100%. The others types of controls (tridimensional) shall be in conformance with IPC-6012 (§4).

12.2 PCB QUALIFICATION:

The suppliers has to qualify all new products, new issue, major process change or manufacturing facility change. They may be asked to perform a periodic qualification that will be specified for each product. The qualification methodology depends on the final application of the product:

Sector	Qualification methodology
Aeronautic/Aerospace/defense	FAI according AS/EN 9102
Automotive	PPAP level 3 according to AIAG IMDS declaration is required as a part of the PPAP
Others	Pre serial Qualification report

Qualification must be performed as same conditions of the mass production.

The first batch must be delivered with the following documents:
- Material list (base material data sheet, batch number, certificate of conformity) following the stack
- Solder resist data sheet
- Finish(es) references
- Subcontracted operation list and name of subcontractors
- Certificate of conformity
- Test certificates
- Delivery order with the purchase order, reference, quantity and PCB's date code
- Control report with following information
- Coupon (micro section after thermal shock and with representative vias)

Dimensional control
- Length, width and thickness of PCBs
- Bow and twist
- Functional dimensions, center-to-center distances, trimming and chamfering
- Line width, spacing and isolation
- Hole size and positioning
- Finishes thickness with X-ray fluorescence ; at least 5 thickness measurements by panel (min, max and standard deviation)

Circuit Visual inspection
- Centering and stack layers
- Base material surface/ subsurface aspect
- Conductor/pad/land aspects
- Plated through/unsupported hole aspect
- Marking
- Solder mask aspect
- Finish type and aspect

Microsection :

- Layer to layer spacing, layer thickness
- Annular ring
- Copper foil thickness (internal and surface layers)
- Copper plating thickness – hole wall(6 points measurement)
- Conductor spacing measurement
- Micro section photo after thermal shock

Electrical test
- Continuity test, isolation test and related test parameters

Others
- Ionic contamination
- Tape test (Solder mask adherence test)
- Solderability testing
- Solder sample, segregated from other product, with "S/S" written large (covering more than 50%) marker on BOTH sides of the PCB
- Impedance test (if applicable)

12.3 NEXT BATCHES

Following documents will, at least, be attached to the next deliveries:
- **Certificate of conformance** (compliance with ISO 17050-1 and ISO 17050-2 or specific requirement)
- **Dimensional control** :
  - Length, width, functional dimensions and circuit board thickness
  - Drilling conformance
  - Twist conformance
  - Trimming conformance
  - Finish thickness with X-ray fluorescence (min and max)
- **Visual inspection conformity**:
  - Centering and layer stack
  - Base material surface/ subsurface aspect
  - Centering and copper aspect
  - Plated through/unsupported hole aspect
  - Solder mask aspect and marking
  - Finish type and aspect
- **Micro section**:
  - Layer stack conformity : material thickness, layer centering
  - Copper plating thickness – hole wall(6 points measurement)
  - Plated hole conformity
  - Representative picture
- **Electrical test**:
  - Test certificate
- **Others**:
  - Ionic contamination
  - Tape test conformity
  - Base material reference
  - Solderability test conformity

13.**ARCHIVING**

Supplier must archive manufacturing tracking sheets, all documents listed in chap 12 and the coupons which have undergone thermal shocks at least for 15 years or according to the specified duration.